IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
Before the Board of Patent Appeals and Interferences

In re Patent Application of: SUGA
Serial No. 09/898,082
Filed: July 5, 2001
Title: SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE DEVICE

Atty Dkt. 925-203
C# M#
Group Art Unit: 2815
Examiner: Nguyen, Joseph H.
Date: April 21, 2003

Assistant Commissioner for Patents
Washington, DC 20231

Sir:

☐ **Correspondence Address Indication Form Attached.**

☐ **NOTICE OF APPEAL**
Applicant hereby appeals to the Board of Appeals from the decision dated _____ of the Examiner twice/finally rejecting claims _____ ($ 320.00) $

☒ An appeal **BRIEF** is attached in triplicate in the pending appeal of the above-identified application ($ 320.00) $ 320.00

☐ Credit for fees paid in prior appeal without decision on merits -$ ( )

☐ A reply brief is attached in triplicate under Rule 193(b) **(no fee)**

☐ Petition is hereby made to extend the current due date so as to cover the filing date of this paper and attachment(s) **($110.00/1 month**; $410.00/2 months; **$930.00/3 months**; $1450.00/4 months) $

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☐ "Small entity" statement attached.

SUBTOTAL $ 320.00

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Any future submission requiring an extension of time is hereby stated to include a petition for such time extension. The Commissioner is hereby authorized to charge any deficiency, or credit any overpayment, in the fee(s) filed, or asserted to be filed, or which should have been filed herewith (or with any paper hereafter filed in this application by this firm) to our **Account No. 14-1140.** A duplicate copy of this sheet is attached.

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For: SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE DEVICE

* *

April 21, 2003

Assistant Commissioner for Patents
Washington, DC 20231

APPEAL BRIEF

Sir:

Applicant hereby appeals the Final Rejection of August 21, 2002, Paper No. 7.

REAL PARTIES IN INTEREST

The real parties in interest are (a) Sharp Kabushiki Kaisha, (b) Oki Electric Industry Co., Ltd., (c) Sanyo Electric Co., Ltd., (d) Sony Corporation, (e) Kabushiki Kaisha Toshiba, (f) NEC Corporation, (g) Hitachi, Ltd., (h) Fujitsu Limited, (i) Matsushita Electric Industrial Co., Ltd., (j) Mitsubishi Denki Kabushiki Kaisha, and (k) Rohm Co., Ltd., all corporations of the country of Japan. The instant application is assigned to these entities (a)-(k).

RELATED APPEALS AND INTERFERENCES

The appellant, the undersigned, and the assignee are not aware of any related appeals or interferences which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

STATUS OF CLAIMS

Claims 1, 3-9 and 20-24 are pending and have been rejected. No claims have been substantively allowed.

STATUS OF AMENDMENTS

No amendments have been filed since the date of the Final Rejection. However, a Response After Final filed December 23, 2002 was considered by the Examiner as evidenced by the Advisory Action dated January 17, 2003.

Additionally, an Information Disclosure Statement and Assignment have been filed herewith.

SUMMARY OF INVENTION

For purposes of example and without limitation, certain example embodiments of the instant invention relate to a semiconductor device including first and second portions which are solid state bonded to each other. Referring to Figures 3-4 of the instant application, for example, the first portion 100 includes a semiconductor substrate 1 which supports a wiring layer 3, insulating layer 7, and conductive regions 5, 6. Conductive region 5 is provided in a through-hole 13 defined in insulating layer 7, while conductive

region 6 is in the form of a wiring layer provided on top of insulating layer 7. Because of chemical mechanical polishing (CMP) for example, the exposed surfaces of conductive regions 5, 6 are at least partially concave in shape so as to define dishing portions (e.g., see reference numeral 17 in Fig. 3 which indicates a dishing portion). In this first portion 100, etching (e.g., RIE) as shown in Figures 2a-2c is used in order to lower the exposed surface of through hole insulating portion(s) 11 relative to the exposed surface of conductive regions 5, 6. As a result, at least part of the exposed concave surfaces of conductive regions 5, 6 protrude outwardly from the exposed surface of through hole insulator region 11 as shown in Fig. 3.

The second portion 200 is formed in a similar manner. Fig. 3, for example, illustrates that the second portion includes semiconductor substrate 20 which supports a wiring layer 23, insulating layer 27, and conductive regions 25, 26. Conductive region 25 is provided in a through-hole 28 defined in insulating layer 27, while conductive region 26 is in the form of a wiring layer provided on top of insulating layer 27. Because of chemical mechanical polishing (CMP) for example, the exposed surfaces of conductive regions 25, 26 are at least partially concave in shape so as to define dishing portions (e.g., see reference numeral 29 in Fig. 3 which indicates a dishing portion).

Then, as shown in Figures 3-4, the first portion 100 and second portion 200 are pressed together using force F in order to solid state bond the concave shaped dishing portion(s) of conductive regions 5, 6 of the first portion 100 *directly* to the dishing portions of conductive regions 25, 26 of the second portion 200 (e.g., pg. 13, lines 1-15). As shown in Fig. 4, a clearance (or gap) 30 may be left between the first portion 100 and second portion 200 in areas adjacent the respective through hole insulator regions 11, 21

where no conductive region is provided. Accordingly, the conductive regions are securely and/or directly bonded *directly* to each other even though the dishing portions were initially provided in these conductive regions. As a result of this technique, an advantage is that a high reliability electrical connection of the conductive regions can be realized (see page 7, lines 5-13; and page 13, lines 18-21).

The concave dishing portions 17, 29 shown in Fig. 3 are present at the respective surfaces of conductors 5, 6, 25 and 26 *before* the conductors are solid-state bonded to one another. After the conductors are solid-state bonded to one another as shown in Fig. 4, these dishing portions need not be present in the final product. However, it is well known in the art that *one of ordinary skill can tell from examining the final product (e.g., see Fig. 4) whether or not the claimed process of bonding two opposed concave dishing portions to one another (e.g., see Fig. 3) was used in making the final product.* In particular, in the final product, peripheral and central parts of solid-state bonded dishing portions are different in strain and texture due to the difference between deformation rates of the central and peripheral parts of the dishing portions – even when the dishing portions do not exist in the final product. When dishing portions were used, in the final product the strain is concentrated in the peripheral parts of the bonded dishing portions, and thus the peripheral parts of the dishing portions are more strongly bonded. In other words, it is clear that one can tell from an examination of the final product whether opposed concave dishing portions were solid-state bonded to one another.

ISSUES

1. Whether claims 1, 3-9 and 20-24 are unpatentable under 35 U.S.C. Section 102(b) over Kawai (U.S. Patent No. 5,939,789).

GROUPING OF CLAIMS

The claims are divided into the following separate and distinct claims groups, each of which stands/falls on its own regardless of any other group:

A. Claims 20, 22 and 24.

B. Claim 21.

C. Claim 23.

D. Claims 1, 3, 4, 7 and 9.

E. Claim 5.

F. Claims 6 and 8.

The reasons why each of the aforesaid Groups stands/falls on its own independent of the other groups are set forth below where each Group is discussed.

ARGUMENT

It is axiomatic that in order for a reference to anticipate a claim, it must disclose, teach or suggest each and every feature recited in the claim. See, e.g., Kalman v. Kimberly-Clark Corp., 713 F.2d 760, 218 USPQ 781 (Fed. Cir. 1983). The USPTO has the burden in this respect. As will be shown herein, Kawai fails to disclose or suggest each and every feature of the claimed inventions, and thus fails to anticipate the claims.

A. Claim 20 (claims 22 and 24 stand/fall therewith).

Claim 20 stands rejected under 35 U.S.C. under 35 U.S.C. Section 102(b) as being allegedly anticipated by Kawai. This Section 102(b) rejection should be reversed for at least the following reasons.

Claim 20 requires "a first substrate supporting a first insulating layer with a contact hole defined therein, and a first conductive material filling in the contact hole in the first insulating layer and protruding above a surface of the first insulating layer; a second substrate supporting a second insulating layer with a contact hole defined therein, and a second conductive material filling in the contact hole in the second insulating layer; and wherein the first conductive material that fills in the contact hole in the first insulating layer and the second conductive material that fills in the contact hole in the second insulating layer are solid-state-bonded to each other so as to contact one another in a bonded state."

For example, see Fig. 4 of the instant application which illustrates that the conductive material 5 in contact hole 13 of insulating layer 7 is solid-state-bonded to and ***contacts*** the conductive material 25 provided in through hole 28 of the other insulating layer 27. Moreover, Figs. 3-4 of the instant application illustrate that the conductive materials 5 and 25 each protrude above their corresponding insulating layers 7 and 27, respectively. Kawai fails to disclose or suggest the aforesaid quoted and underlined aspects of claim 20.

The Final Rejection relies on Fig. 12(c) of Kawai. Kawai in Fig. 12(c) illustrates insulting films 1 having holes 4 defined therein which are filled with copper (Cu). Moreover, tin (Sn) bonding members 5 and metal wirings 2 are provided between the insulating films. Kawai's requirement of tin bonding members 5 and metal wirings 2

means that in Kawai the Cu material which fills opposed through holes 4 in Kawai is *not* directly bonded to each other and thus is in *non*-contacting relation. In other words, in direct contrast with the requirement of claim 20, in Kawai the conductive materials in different holes 4 are not in contact with one another. Bonding members 5 and metal wirings 2 prevent such conductive materials in holes 4 from contacting one another in Kawai – teaching directly away from the invention of claim 20. Kawai is entirely unrelated to the invention of claim 20 and cannot possibly anticipate the same.

During the Interview reflected by the Interview Summary dated December 6, 2002, the Examiner argued that "contact" as recited in the next-to-last line of claim 20 does not mean "directly contact." Thus, the Examiner argued that in Fig. 12(c) of Kawai the Cu in one hole 4 contacts the Cu in another hole 4 even though layers 2 and 5 are therebetween. The Examiner is wrong. The word "contact" means touching. The Examiner's argument that "contact" does not mean touching is illogical and defies the clear and well known meaning of the word "contact." The Examiner's interpretation of the claimed word "contact" is not reasonable.

Furthermore, Fig. 12(c) of Kawai also fails to disclose or suggest the requirement of claim 20 of a "first conductive material filling in the contact hole in the first insulating layer and protruding above a surface of the first insulating layer." In Fig. 12(c) of Kawai, Cu in a hole 4 is not "protruding above" a surface of a corresponding insulating layer 1. Instead, the top surface of Cu material in a hole 4 is flush with the top surface of insulating layer 1. Moreover, it cannot be said that Sn bonding members 5 meet this aspect of claim 20, because Sn bonding members 5 are not the material filling a contact

hole as required by claim 20 (Sn and Cu are clearly different materials). Again, Kawai is entirely unrelated to the invention of claim 20 in this respect.

Since Kawai fails to disclose or suggest each of the two aspects of claim 20 discussed above, the Section 102(b) rejection of claim 20 should be reversed.

B. Claim 21.

Claim 21 also stands rejected under Section 102(b) over Kawai. This Section 102(b) rejection should be reversed for at least the following reason.

In addition to the reasons discussed above with respect to claim 20, claim 21 further requires that "the *second* conductive material filling in the contact hole in the second insulating layer protrudes above a surface of the second insulating layer." For example, Figs. 3-4 of the instant application illustrate that conductive material 5 and 25 filling respective contact holes 13 and 28 in the insulating layers, protrude above the respective surfaces of insulating layers 7 and 27.

In Fig. 12(c) of Kawai, Cu 4 does not protrude above a surface of a corresponding insulating layer 1. Instead, the top surface of Cu material in a hole 4 is flush with the top surface of insulating layer 1. Moreover, it cannot be said that Sn bonding members 5 meet this aspect of claim 20, because Sn bonding members 5 are not the material filling a contact hole as required by claim 21 (Sn and Cu are clearly different materials). Again, Kawai is entirely unrelated to the invention of claim 21 in this respect.

C. Claim 23.

Claim 23 also stands rejected under Section 102(b) over Kawai. This Section 102(b) rejection should be reversed for at least the following reason.

In addition to the reasons discussed above with respect to claim 20, claim 23 further requires that "*concave* surfaces of the respective first and second conductive materials are bonded to one another so as to contact each other." For example, see Fig. 3 of the instant application which illustrates that the respective surfaces of conductors 5 and 25 are *concave* in shape. These surfaces are concave in shape before bonding, but need not be concave in shape after bonding.

The BPAI has held that "if the record reflects an advantage or unobvious difference between the claimed product and the prior art product, then the product-by-process rationale for rejecting the claim must be withdrawn." *In re Swirbel*, 2002 WL 1801019, Appeal No. 2000-0314 (BPAI 2002) (copy attached hereto). *See also In re Marosi*, 218 USPQ 289, 292-93 (Fed. Cir. 1983). Listed below are clear unobvious differences between the claimed product and the cited art, which necessitate reversal of the rejection.

As explained above, one can tell from examining the final product (e.g., see Fig. 4) whether or not the claimed process of bonding two opposed concave portions to one another was used in making the final product. In particular, in the final product, peripheral and central parts of solid-state bonded concave portions are different in strain and texture due to the difference between deformation rates of the central and peripheral parts of the concave portions – even when the concave portions do not exist in the final product. When concave portions were used, in the final product the strain is concentrated in the peripheral parts of the bonded portions, and thus the peripheral parts of the portions are *more strongly bonded.* This represents a significant unexpected advantage over the

cited art. Accordingly, it is respectfully submitted that the Examiner should consider the "concave" aspect of this claim.

As explained above, in Kawai holes 4 are filled with Cu (e.g., col. 7, lines 48-50). However, in contrast with claim 23, Kawai fails to disclose or suggest that the surface of any Cu member in a hole 4 is concave in shape. Thus, Kawai cannot meet the invention of claim 23.

D. Claim 1(claims 3, 4, 7 and 9 stand/fall therewith)

Claim 1 also stands rejected under Section 102(b) as being allegedly anticipated by Kawai. This Section 102(b) rejection should be reversed for at least the following reasons.

Claim 1 requires "a first portion comprising a first substrate, a conductive layer and an insulating layer laminated on the first substrate and a bonding surface that is chemically mechanically polished and exposes a conductive region and an insulating region, wherein the conductive region includes a concave surface defining a dishing portion; a second portion comprising a second substrate, a conductive layer and an insulating layer laminated on the second substrate and a bonding surface that is chemically mechanically polished and exposes at least a conductive region having a concave surface defining a dishing portion; and wherein the bonding surface of the first portion and the bonding surface of the second portion are solid-state-bonded to each other so that the dishing portions of the conductive regions of the respective first and second portions are bonded to each other so as to contact one another, and at least one of the bonding surface of the first portion and the bonding surface of the second portion has the insulating region lowered with respect to the conductive region." For example, see Fig. 3

of the instant application which illustrates opposing concave dishing portions 17, 29 which are to be solid state bonded to one another.

Kawai fails to disclose or suggest the concave surface dishing portions of claim 1. Kawai in Fig. 12(c) illustrates Cu filled through holes 4 provided in insulating films 1, which are in electrical communication with one another via metal wirings 2 and Sn bonding members 5. However, Kawai differs from the invention of claim 1 in that the Cu material which fills through holes 4 in Kawai *does not have a dishing portion (i.e., it has no concave shaped surface)*. Furthermore, the Sn bonding members 5 and metal wirings 2 in Fig. 12(c) of Kawai also have no concave dishing portions on respective surfaces thereof. Since Kawai fails to disclose or suggest the claimed dishing portions, claim 1 cannot be anticipated by Kawai.

The Examiner *admits* that the concave dishing portions recited in claim 1 are not disclosed or suggested by Kawai. However, the Examiner argues that the claimed dishing portions can be ignored because they are part of a process portion of a *product-by-process* claim. Claim 1 does not state that the final product must include the dishing portions; instead, claim 1 states that two opposed concave dishing portions are bonded to one another in order to form the final product. Thus, as acknowledged by both the Examiner and the applicant, the final product need not have the claimed concave dishing portions.

Where the Examiner and applicant disagree is on the issue of whether the claimed concave dishing portions must be considered by the Examiner in the context of product-by-process claim 1. The Examiner feels that the dishing portions can be ignored since they are recited in the context of a product-by-process, whereas applicant believes that

the dishing portions should be considered since they are a positively recited limitation which lead to unobvious differences in the final product and since one of skill in the art can tell from examining the final product whether the dishing portions were used in the process of manufacture.

The BPAI has held that "if the record reflects an advantage or unobvious difference between the claimed product and the prior art product, then the product-by-process rationale for rejecting the claim must be withdrawn." *In re Swirbel*, 2002 WL 1801019, Appeal No. 2000-0314 (BPAI 2002) (copy attached hereto). *See also In re Marosi*, 218 USPQ 289, 292-93 (Fed. Cir. 1983).

In the instant case, the claimed product and that of the cited art are clearly made by different processes which result in different final products. Moreover, the claimed dishing portions result in unobvious differences and advantages over the cited art. In particular, a higher reliability electrical connection of the conductive regions can be realized when the claimed dishing portions are used in the process of manufacture (e.g., page 7, lines 5-13; and page 13, lines 18-21). Further advantageous differences are discussed below with respect to stresses in the resulting final product. According to the well-established law, the Examiner thus "must" withdraw the product-by-process rationale for the rejection and consider the claimed concave dishing portions.

An examination of the final product will indicate whether the claimed dishing portions were used in making the product. In particular, one can tell from examining the final product (e.g., see Fig. 4) whether or not the claimed process of bonding two opposed concave dishing portions to one another (e.g., see Fig. 3) was used in making the final product. In the final product, peripheral and central parts of solid state bonded

dishing portions are different in strain and texture due to the difference between deformation rates of the central and peripheral parts of the dishing portions. In the final product, the strain is concentrated in the peripheral parts of the bonded dishing portions, and thus the peripheral parts of the dishing portions are *more strongly bonded.* This clearly represents an unexpected and unobvious difference with respect to the prior art.

Furthermore, it is well established that with a product-by-process claim, "it remains upon the examiner to show that [the claimed product] reasonably appears to be either identical with or only slightly different than the claimed [product]." *In re Kung*, 17 USPQ2d 1545, 1548 (BPAI 1989). In this case, it is clear that the final product of the cited art was not made using the concave dishing portions required by claim 1. The differences in the final products are clear. For this additional reason, the Section 102(b) rejection should be reversed.

Thus, applicant respectfully submits that the Examiner should consider the concave dishing aspects of claim 1 which the Examiner has admitted are not disclosed or suggested by Kawai. Since the cited art fails to disclose or suggest the claimed dishing portions, the rejection should be reversed.

E. Claim 5.

Claim 5 requires that "the insulating region of the first portion and the insulating region of the second portion are put in contact with or solid-state-bonded to each other." For example, see the instant specification at paragraph [0012].

Kawai clearly fails to disclose or suggest this aspect of claim 5. In Fig. 12(c) of Kawai, different insulators 1 clearly are not in contact with one another, or solid-state bonded to one another. The rejection of claim 5 must be reversed.

F. Claim 6 (claim 8 stands/falls therewith)

Claim 6 requires that "the insulating region that surrounds the conductive region of the first portion and the insulating region that surrounds the conductive region of the second portion are put in contact with or solid-state-bonded to each other."

Again, Kawai fails to disclose or suggest this aspect of claim 6. In Fig. 12(c) of Kawai, different insulators 1 clearly are not in contact with one another, or solid-state bonded to one another. The rejection of claim 6 must be reversed.

CONCLUSION

In conclusion it is believed that the application is in clear condition for allowance; therefore, early reversal of the Final Rejection and passage of the subject application to issue are earnestly solicited.

Respectfully submitted,

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APPENDIX

CLAIMS ON APPEAL

1. A semiconductor device comprising:

a first portion comprising a first substrate, a conductive layer and an insulating layer laminated on the first substrate and a bonding surface that is chemically mechanically polished and exposes a conductive region and an insulating region, wherein the conductive region includes a concave surface defining a dishing portion;

a second portion comprising a second substrate, a conductive layer and an insulating layer laminated on the second substrate and a bonding surface that is chemically mechanically polished and exposes at least a conductive region having a concave surface defining a dishing portion; and wherein

the bonding surface of the first portion and the bonding surface of the second portion are solid-state-bonded to each other so that the dishing portions of the conductive regions of the respective first and second portions are bonded to each other so as to contact one another, and

at least one of the bonding surface of the first portion and the bonding surface of the second portion has the insulating region lowered with respect to the conductive region.

3. A semiconductor device as claimed in claim 1, wherein the conductive region of the first portion and the conductive region of the second portion are solid-state-bonded to each other, and the insulating region of the first portion and the insulating region of the second portion face each other with interposition of a clearance.

4. A semiconductor device as claimed in claim 3, wherein the insulating region that surrounds the conductive region of the first portion and the insulating region that surrounds the conductive region of the second portion face each other with interposition of a clearance.

5. A semiconductor device as claimed in claim 1, wherein the conductive region of the first portion and the conductive region of the second portion are solid-state-bonded to each other, and the insulating region of the first portion and the insulating region of the second portion are put in contact with or solid-state-bonded to each other.

6. A semiconductor device as claimed in claim 5, wherein the insulating region that surrounds the conductive region of the first portion and the insulating region that surrounds the conductive region of the second portion are put in contact with or solid-state-bonded to each other.

7. A semiconductor device as claimed in claim 4, wherein the conductive regions are end surfaces of through hole conductors and the insulating regions are end surfaces of through hole insulators that surround the respective through hole conductors.

8. A semiconductor device as claimed in claim 6, wherein the conductive regions are end surfaces of through hole conductors and the insulating regions are end surfaces of through hole insulators that surround the respective through hole conductors.

9. A semiconductor device as claimed in claim 1, wherein the first substrate or the second substrate is any one of a semiconductor substrate, an inorganic substrate and an organic substrate.

20. A semiconductor device comprising:

a first substrate supporting a first insulating layer with a contact hole defined therein, and a first conductive material filling in the contact hole in the first insulating layer and protruding above a surface of the first insulating layer;

a second substrate supporting a second insulating layer with a contact hole defined therein, and a second conductive material filling in the contact hole in the second insulating layer; and

wherein the first conductive material that fills in the contact hole in the first insulating layer and the second conductive material that fills in the contact hole in the second insulating layer are solid-state-bonded to each other so as to contact one another in a bonded state.

21. The semiconductor device of claim 20, wherein the second conductive material filling in the contact hole in the second insulating layer protrudes above a surface of the second insulating layer.

22. The semiconductor device of claim 20, wherein the first and second conductive materials are of the same material.

23. The semiconductor device of claim 20, wherein concave surfaces of the respective first and second conductive materials are bonded to one another so as to contact each other.

24. The semiconductor device of claim 20, wherein a gap or clearance is defined between the first and second insulating layers adjacent an area where the conductive materials are solid-state-bonded to one another.

Board of Patent Appeals and Interferences

Patent and Trademark Office (P.T.O.)
*1 EX PARTE THOMAS J. SWIRBEL, JOHN K. ARLEDGE, AND JOAQUIN BARRETO
Appeal No. 2000-0314
Application No. 08/944,192

NO DATE REFERENCE AVAILABLE FOR THIS DOCUMENT

MOTOROLA, INC.

INTELLECTUAL PROPERTY DEPARTMENT

8000 WEST SUNRISE BLVD

FT. LAUDERDALE, FL 33322

Before HAIRSTON, BARRETT, and LEVY

Administrative Patent Judges

Hairston

Administrative Patent Judge

ON BRIEF

DECISION ON APPEAL

This is an appeal from the final rejection of claims 1 through 16.

The disclosed invention relates to a multi-layered printed circuit board that has a central core substrate sandwiched between a photoimaged dielectric layer and a non-photoimageable dielectric layer. A metallization pattern separates each of the dielectric layers from the central core substrate. Vias are formed in the photoimaged dielectric layer by a photoimaging process, and vias are formed in the non-photoimageable dielectric layer by a laser drilling process.

Claims 1 and 15 are illustrative of the claimed invention, and they read as follows:

1. A multi-layer printed circuit board, comprising:
a central core substrate having first and second major opposing surfaces containing first and second respective metallization patterns;
a photoimaged dielectric layer deposited on the first surface and overlying the first metallization pattern, said photoimaged dielectric layer containing a third metallization pattern and photoimaged vias that electrically connect the third metallization pattern to the underlying first metallization pattern; and
a non-photoimageable dielectric layer deposited on the second surface and overlying the second metallization pattern, said non-photoimageable dielectric layer containing a fourth metallization pattern and laser-formed vias that electrically connect the fourth metallization pattern to the underlying second metallization pattern.

15. A multi-layer printed circuit board comprising:
a photoimaged dielectric layer on one side of a cental core substrate and a non-photoimaged dielectric layer on an opposite side of the central core substrate, the photoimaged dielectric layer containing electrically conductive vias that are formed by a photolithographic process and the non- photoimaged dielectric layer containing electrically conductive vias that are formed by a laser.

The references relied on by the examiner are:

Ohnuki et al. (Ohnuki)	4,668,332	May 26, 1987
Tsukada et al. (Tsukada)	5,451,721	Sep. 19, 1995
Bhatt et al. (Bhatt)	5,487,218	Jan. 30, 1996
Hoshino [FN1]	8-8541	Jan. 12, 1996

(published Japanese Kokai Patent Application)

*2 Claim 15 stands rejected under 35 U.S.C. § 102(b) as being anticipated by Hoshino.

Claims 1 through 11, 14 and 16 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Tsukada in view of Hoshino.

Claim 12 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Tsukada in view of Hoshino and Bhatt.

Claim 13 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Tsukada in view of Hoshino and Ohnuki.

Reference is made to the brief (paper number 9) and the answer (paper number 10) for the respective positions of the appellants and the examiner.

OPINION

We have carefully considered the entire record before us, and we will reverse the 35 U.S.C. § 102(b) rejection of claim 15, and the 35 U.S.C. § 103(a) rejection of claims 1 through 14 and 16.

Turning first to the anticipation rejection of claim 15, the examiner indicates (answer, page 4) that Hoshino discloses all of the limitations of product claim 15 except for the photolithographic process and the laser process for making the vias [FN2] in the photoimaged dielectric layer and the non- photoimaged dielectric layer, respectively. According to the examiner (answer, page 4), the "presence of process limitations in product claims, which product does not otherwise patentably distinguish over prior art, cannot impart patentability to that product." When the claimed invention is to a product, it is the patentability of that product that is determined, not the method by which it is made. In re Thorpe, 777 F.2d 695, 697, 227 USPQ 964, 966 (Fed. Cir. 1985). If the record reflects an advantage or unobvious difference between the claimed product and the prior art product, then the product-by-process rationale for rejecting the claim must be withdrawn. In re Marosi, 710 F.2d 799, 803, 218 USPQ 289, 292-93 (Fed. Cir. 1983). The admitted prior art (specification, page 1, line 23 through page 2, line 1) and Tsukada (column 1, lines 13 through 16 and 59 through 62) provide evidence of differences between vias formed by three different processes. Vias formed by mechanical drilling are larger than vias formed by photolithographic techniques, and vias formed by the latter technique are larger than vias formed by a laser. A decrease in via size results in a corresponding increase in wiring density of the printed circuit board. An additional advantage of the laser technique for forming vias is that a thicker dielectric can be used in the printed circuit board. In view of the noted advantages of laser formed vias over photolithographically formed vias, the product-by-process reasoning advanced by the examiner can not stand. Thus, the 35 U.S.C. § 102(b) rejection of claim 15 is reversed.

*3 In the 35 U.S.C. § 103(a) rejection of claims 1 through 11, 14 and 16, the examiner used the same product-by-process rationale in connection with the teachings of Hoshino. For all of the reasons expressed supra, this rationale can not stand. Even if the teachings of the two references could be properly combined, the combined teachings would still lack a photoimaged dielectric layer overlying the metallization pattern on one side of the core substrate, and a non-photoimageable dielectric layer overlying the metallization pattern on the other side of the core substrate. In Tsukada, a photoimageable dielectric layer 18 is located over the

metallization patterns on both sides of the core substrate (Figure 2C). In Hoshino, a non- photoimageable dielectric layer 4a is located over the metallization patterns on both sides of the core substrate (Figure 1). As a result thereof, the 35 U.S.C. § 103(a) rejection of claims 1 through 11, 14 and 16 is reversed.

The 35 U.S.C. § 103(a) rejection of claims 12 and 13 is reversed because the teachings of Bhatt and Ohnuki do not cure the noted shortcomings in the teachings of Tsukada and Hoshino.

DECISION

The decision of the examiner rejecting claim 15 under 35 U.S.C. § 102(b) is reversed, and the decision of the examiner rejecting claims 1 through 14 and 16 under 35 U.S.C. § 103(a) is reversed.

REVERSED

BOARD OF PATENT APPEALS AND INTERFERENCES

KENNETH W. HAIRSTON

Administrative Patent Judge

LEE E. BARRETT

Administrative Patent Judge

STUART S. LEVY

Administrative Patent Judge

FN1. A copy of the translation of this reference is attached.

FN2. Hoshino indicates (translation, pages 6, 14, 17, 18 and 21) that the vias in the two dielectric layers are formed by chemical means.

2002 WL 1801019 (Bd.Pat.App & Interf.)

END OF DOCUMENT